IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Ting, *et al.*	Docket No.:	TSM03-0945
Serial No.:	10/840,125	Art Unit:	2811
Filed:	May 6, 2004	Examiner:	Ori Nadav

For: Notched Spacer for CMOS Transistors

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Appellant appeals the final rejection of claims 16-28. This brief is filed within one month of the Notice of Panel Decision on Pre-Appeal Brief Review, mailed on December 10, 2007, and is in furtherance of the Notice of Appeal, filed on October 12, 2007.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party in Interest
II. Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims Appendix
IX. Evidence Appendix
X. Related Proceedings Appendix

I. Real Party in Interest

The present application is assigned to Taiwan Semiconductor Manufacturing Co., Ltd. ("TSMC"), the real party in interest.

II. Related Appeals and Interferences

There are no other appeals, interferences, or judicial proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. Status of Claims

Claims 16-28 are pending and stand finally rejected. Claims 1-15 were cancelled. Claims 29-33 were withdrawn. The final rejection of each of claims 16-28 is being appealed.

IV. Status of Amendments

Appellant filed a Response under 37 C.F.R. § 1.116 on September 11, 2007, in which no amendments were made to the claims. Appellant filed a Notice of Appeal along with a Request for Pre-Appeal Review on October 12, 2007. The Pre-Appeal review board indicated that the application was to remain under appeal, in a Notice of Panel Decision, dated December 12, 2007. Appellant files this Appeal Brief in response to the review panel's decision.

V. Summary of Claimed Subject Matter

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the

claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

With regard to independent claim 16, a method of forming a semiconductor device is provided (*see Paragraphs 0009, 0010, 0011, and 0012*). A gate electrode 122 is formed on a substrate 110 (*see Figures 1B-1I and Paragraphs 0009, 0010, 0011, 0012, 0020*), the substrate 110 having a first conductivity type (*see Paragraphs 0016 and 0017*). A notched spacer 132 is formed alongside the gate electrode 112 (*see Figures 1E-1I and Paragraphs 0010, 0024, 0025*) such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate 132 (*see Figures 1D, 1E, and Paragraphs 0010, 0024, 0025)*, the notched spacer 132 comprising a single homogenous layer (*see Paragraphs 0021, 0023, 0026, and 0027*). A first ion implant is performed (*see Figure 1F and Paragraphs 0027, 0028, 0029)* wherein only the gate electrode 120 and the notched spacer 132 act as masks during the first ion implant (*see Figure 1F and Paragraph 0027*), the first ion implant using ions of the first conductivity type (*see Paragraph 0028*). One or more second ion implants are performed using ions of a second conductivity type (*see Figures 1G, 1I, and Paragraphs 0030, 0031, 0032*).

With regard to independent claim 24, a method of forming a semiconductor device is provided (*see Paragraphs 0009, 0010, 0011, and 0012)*. A gate electrode 122 is formed on a substrate 110 (*see Figures 1B-1I and Paragraphs 0009, 0010, 0011, 0012, 0020*), the substrate having a first conductivity type (*see Paragraphs 0016 and 0017)*. A first layer 126 is formed over the substrate 110 and the gate electrode 122 (*see Figure 1C, 1D, and Paragraph 0021, 0023, 0024, 0025*). A second layer 128 is formed over the first layer 126 (*see Figure 1C and paragraphs 0021, 0022, and 0023)*. A portion of the second layer is removed such that a spacer mask 130 is formed on the first layer 126 on a side of the gate electrode 122 (*see Figures 1D, 1E, and Paragraph 0023, 0025, and 0027*). The first layer 126 is etched to form a notched spacer 132 wherein the spacer mask 130 acts as a mask (*see Figures 1D, 1E and Paragraphs 0024, 0025)*, the etching process removes at least a portion of the first layer 126 along a surface of the substrate 110 (*see Paragraphs 0010, 0024, 0025*), thereby forming a notch in the notched spacer

132 alongside the gate electrode 122 near the substrate 110 (*see Figures 1E, 1F, 1H, 1I, and Paragraphs 0010, 0024, 0025, and 0026*). The spacer mask 130 is removed (*see Figure 1F and Paragraph 0027)*. A first ion implant is performed after the spacer mask has been removed (*see Figure 1F, and Paragraph 0028*), the first ion implant uses ions of the first conductivity type (*see Paragraph 0028)*. One or more second ion implants is performed using ions of a second conductivity type (*see Figures 1G, 1I, and Paragraphs 0030, 0031, 0032*).

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 16-28 are unpatentable under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

VII. Argument

Rejection of independent claim 16 and dependent claims 17-23.

Claim 16, and, by dependence, claims 17-23 require "forming a notched spacer alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate". The Examiner asserted, in Final Office Action dated July 12, 2007, that "the step of forming a notched spacer alongside the gate electrode, 'such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate' is not taught in the specification as originally filed." However, there is clear support for this claim element in Figures 1D and 1E and Paragraphs 0010, 0024, and 0025 of the specification as originally filed.

Paragraph 0010 states, "... a notched spacer is formed alongside the gate electrode such that a portion of the notched spacer is completely, or partially removed along the corner formed between the surface of the substrate and the gate electrode sidewall." Clearly, a notched spacer

partially removed along the corner formed between the surface of the substrate and the gate electrode is "thinner near the substrate."

The Examiner states that the specification "says nothing about the thickness of the portion of the dielectric layer that remains, and does not teach the thickness of the spacer is thinner near the substrate." Moreover, the Examiner states, "Claim 16, as originally filed, says that a notched spacer is formed that is, "thinner along the surface of the substrate," which is not entirely clear (and appears to describe an L-shaped spacer)." (Office Action dated July 12, 2007.)

Appellant disagrees with the Examiner's assertions. To those of ordinary skill in the art, it is obvious that a notched area is a thinner area, not a thicker area. The ordinary and plain meaning of the word "notched" means an indentation, not a protrusion. Therefore, along the surface of the substrate cannot mean an "L-shaped spacer" as the Examiner alleges. Paragraph 0025 and Figures 1D and 1E are reproduced below for the convenience of the Board.

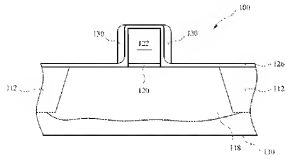

FIG. 1D

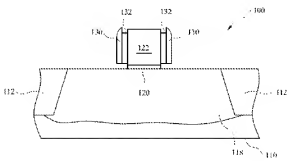

FIG. 1E

Originally filed Figures 1D and IE.

> As illustrated in FIG. 1E, the portion of the first dielectric layer 126 (FIG.1D located under the notched-spacer masks 130 is removed due to the isotropic etching process, thereby creating a notched spacer. The width of the notch will be dependent upon the thickness of the first dielectric layer 126 and the

> notch height may be controlled by varying the etch duration. Furthermore, FIG. 1E illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122. In other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122. This may be desirable, for example, when it is preferred to control the depth and angle of the implant or to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes.

Originally filed paragraph 0025. [Emphasis added.]

As Paragraph 0025 states, "the notch height may be controlled by varying the etch duration." The layer 126 (for example SiO_2) alongside the gate electrode near the substrate is not protected by a mask; therefore, it is easily recognized, by one of ordinary skill in the art, that it is the thickness and thinness of the notched spacer alongside the gate electrode near the substrate, that is controlled by varying the etch duration. Those of ordinary skill in the art will further understand that the portion of the first dielectric layer 126 (the notch height), located under the notched-spacer masks 130 may remain on the side of the gate electrode 122. An isotropic etch tends to clear the thickest portion of a dielectric layer last. Thus, it follows that an etch of relatively short duration may leave a portion of dielectric layer 126 on the lower portion of the side of the gate electrode 122, and an etch of relatively long duration may leave substantially no portion of layer 126 alongside the gate electrode near the substrate.

Therefore, within the specification as originally filed is the description of a method to control the thickness of the notch alongside the gate electrode near the substrate. The Examiner's allegation that the claim element "such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate," is not taught in the specification is incorrect.

Moreover, it is clear to one of ordinary skill in the art that 1) the spacer is alongside the gate electrode, 2) the area of the spacer that is unprotected by the mask is the area of the spacer

that is etched, and 3) the area of the spacer that is unprotected by the mask is along the surface of the substrate. Therefore, to one of ordinary skill in the art, thinner along the surface of the substrate does indeed state that the notched spacer is thinner alongside the gate electrode near the substrate. Amended claim 16, reciting, "forming a notched spacer alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate," is supported at least by original Paragraphs 0010 and 0025.

Further, even if the board finds that claim 16 is not sufficiently supported in the original specification, MPEP 608.01(l) states, "In establishing a disclosure, applicant may rely not only on the description and drawing as filed, but also on the original claims if their content justifies it." Original claim 16 as originally filed recites in part, "forming a notched spacer alongside the gate electrode such that the notched spacer is thinner along the surface of the substrate …," and accordingly, provides the necessary support for amended claim 16 which states, "forming a notched spacer alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate…."

Thus, amended claim 16, and dependent claims 17-23 are supported by the original specification in paragraphs 0010, 0025 and Figures 1D and 1E. Appellant respectfully traverses the rejection of claim 16. Since claims 17-23 depend from claim 16, the same arguments as the independent claim 16 apply to these dependent claims. Therefore, the rejection of claims 17-23 has been traversed.

Rejection of independent claim 24 and dependent claims 25-28.

Claim 24, and, by dependence, claims 25-28 require "etching the first layer to form a notched spacer wherein the spacer mask acts as a mask, the etching process removing at least a

portion of the first layer along a surface of the substrate, thereby forming a notch in the notched spacer alongside the gate electrode near the substrate."

The Examiner has asserted, "There is no support in the specification for removing 'a portion' of the first layer along the substrate." Further, the Examiner states, "The figures and specification as originally filed teach to remove all of the first layer that lies along the substrate, and not simply a portion." (Final Office Action dated July 12, 2007).

Appellant disagrees with the Examiner; there is indeed clear support in the specification for removing "a portion" of the first layer along the substrate. Paragraph 0010 states, "... a notched spacer is formed alongside the gate electrode such that a portion of the notched spacer is completely, or partially removed along the corner formed between the surface of the substrate and the gate electrode sidewall." Clearly, a notched spacer partially removed along the corner formed between the surface of the substrate and the gate electrode has removed "at least a portion of the first layer along a surface of the substrate."

Further, Paragraph 0025 states that while "FIG. 1E illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122[, i]n other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122." (Emphasis added.)

Claim 24 recites, "removing at least a portion" of the first layer. Original figures 1D and 1E, reproduced above, clearly show that "at least a portion" of first layer 126 has been removed. In the illustrated example, "at least a portion" has included the entire portion of layer 126, which is alongside gate electrode 120 and near the surface of substrate 110. Because the phrase "at least a portion" encompasses "all," the original figures provide full and enabling support for claim 24. For this reason alone, the claim limitation of "removing at least a portion of the first layer" is fully disclosed and supported.

Paragraph 0010 refutes the Examiner's allegation that "complete" removal was the only disclosed embodiment in stating, "that a portion of the notched spacer is completely or partially removed." Furthermore, original Paragraph 0025 clearly rebuts the Examiner's contention that "complete" removal was the only disclosed embodiment. Original Paragraph 0025 states, "FIG. 1E illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122. In other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122" (emphasis added). Obviously, if "a portion" of layer 126 remains, then only a portion has been removed.

Furthermore, a review of figure 1E demonstrates that the region of dielectric layer 126 being discussed is the region along the surface of the substrate (which must be the case because the upper region of the layer is covered by mask 130 and thus could not be partially or fully removed). Moreover, original Paragraph 0025 continues, "This may be desirable, for example, when it is preferred to control the depth and angle of the implant or to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes." Those of ordinary skill in the art will understand that the area being discussed in the original specification is "at least a portion of the first layer along a surface of the substrate" and "alongside the gate electrode near the substrate," because only there can the gate dielectric 120 be protected during an etching process. Since it is clear that the specification is referring to the portion of the first layer alongside the gate electrode near the substrate and that "in other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122" (original Paragraph 0025), it is clear that amended claim 24 is supported by original Paragraphs 0010, 0025, Figure 1D and Figure 1E.

Therefore, the element in claim 24 of "removing at least a portion of the first layer along a surface of the substrate, thereby forming a notch in the notched spacer alongside the gate electrode near the substrate" is supported in the specification.

For the above reasons, the rejection of claim 24 is also traversed. Since no independent ground was provided for rejecting claims 25-28, which depend from claim 24, the same arguments as the independent claim 24 apply to these dependent claims. The rejection of claims 25-28 has been traversed.

The originally filed disclosure reasonably conveys to those of ordinary skill in the art that Appellant invented processes including those limitations recited in the claims. Appellant respectfully requests that the final rejection of claims 16-33 be withdrawn and the present application be passed to allowance.

A reversal of the final rejection of claims 16-28 is earnestly requested.

Respectfully submitted,

January 10, 2008
Date

/Mary Adams-Moe/
Mary Adams-Moe
Attorney for Appellant
Reg. No. 57,883

SLATER & MATSIL, L.L.P.
17950 Preston Rd.
Suite 1000
Dallas, Texas 75252
Tel. 972-732-1001
Fax: 972-732-9218

VIII. Claims Appendix

1. 1-15. (Cancelled)

16. (Previously Presented) A method of forming a semiconductor device, the method comprising:

forming a gate electrode on a substrate, the substrate having a first conductivity type;

forming a notched spacer alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate, the notched spacer comprising a single homogenous layer;

performing a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type; and

performing one or more second ion implants using ions of a second conductivity type.

17. (Previously Presented) The method of claim 16, wherein the step of forming a notched spacer comprises forming a first layer and a second layer, forming a mask out of the second layer on the first layer such that the first layer alongside the gate electrode is covered by the mask, etching the first layer such that the first layer along a surface of the substrate next to the gate electrode is removed, and removing the mask.

18. (Original) The method of claim 17, wherein the mask is formed of silicon nitride.

19. (Original) The method of claim 17, wherein the mask is formed of silicon oxide.

20. (Original) The method of claim 16, wherein the step of performing a first ion implant is performed by implanting ions at an oblique angle to the substrate such that impurities of the first conductivity type are implanted in the substrate below the gate electrode.

21. (Previously Presented) The method of claim 16, wherein the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.

22. (Original) The method of claim 16, wherein the notched spacer is formed of silicon dioxide.

23. (Original) The method of claim 16, wherein the notched spacer is formed of silicon nitride.

24. (Previously Presented) A method of forming a semiconductor device, the method comprising:

forming a gate electrode on a substrate, the substrate having a first conductivity type;

forming a first layer over the substrate and the gate electrode;

forming a second layer over the first layer;

removing a portion of the second layer such that a spacer mask is formed on the first layer on a side of the gate electrode;

etching the first layer to form a notched spacer wherein the spacer mask acts as a mask, the etching process removing at least a portion of the first layer along a surface of the substrate, thereby forming a notch in the notched spacer alongside the gate electrode near the substrate;

removing the spacer mask;

performing a first ion implant after the spacer mask has been removed, the first ion implant using ions of the first conductivity type; and

performing one or more second ion implants using ions of a second conductivity type.

25. (Original) The method of claim 24, wherein the step of performing a first ion implant is performed by implanting ions at an oblique angle to the substrate such that impurities of the first conductivity type are implanted in the substrate below the gate electrode.

26. (Original) The method of claim 24, wherein the step of performing one or more second ion implants are performed at an angle normal to the surface of the substrate.

27. (Original) The method of claim 24, wherein the first layer is formed of silicon dioxide.

28. (Original) The method of claim 24, wherein the second layer is formed of silicon nitride.

29. (Withdrawn) A method of forming a semiconductor device, the method comprising:

forming a gate electrode on a substrate, the substrate having a first conductivity type;

forming a first layer over the substrate and the gate electrode;

forming a second layer over the first layer;

removing a portion of the second layer such that a spacer mask is formed on the first layer on a side of the gate electrode;

etching the first layer to form a notched spacer wherein the spacer mask acts as a mask, the etching removing substantially all of a portion of the first layer along a surface of the substrate adjacent the gate electrode;

removing the spacer mask;

performing a first ion implant after the spacer mask has been removed, the first ion implant using ions of the first conductivity type; and

performing one or more second ion implants using ions of a second conductivity type.

30. (Withdrawn) The method of claim 29, wherein the step of performing a first ion implant is performed by implanting ions at an oblique angle to the substrate such that impurities of the first conductivity type are implanted in the substrate below the gate electrode.

31. (Withdrawn) The method of claim 29, wherein the step of performing one or more second ion implants are performed at an angle normal to the surface of the substrate.

32. (Withdrawn) The method of claim 29, wherein the first layer is formed of silicon dioxide.

33. (Withdrawn) The method of claim 29, wherein the second layer is formed of silicon nitride.

IX. Evidence Appendix

No evidence has been relied upon in this appeal.

X. Related Proceedings Appendix

Appellant is unaware of any related appeals or interferences.